Invited Paper: mmMoReEdge: A mmWave Modular and Reconfigurable Testbed Design using a Smart Edge Framework

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***Abstract*— As the complexity of hardware (sensors, components, antennas) and software (algorithms) increases, it is practical and efficient to manage and process test configuration and data analysis as close to the testbed as possible (inline) instead of offline compute platforms. We present mmMoReEdge, a mmWave modular and reconfigurable testbed inspired by a smart edge networking and communication framework, typically found in IoT devices. In mmMoReEdge, complex signal processing is performed on the edge (local servers in close proximity) of a group of testbed nodes. mmMoReEdge offers modularity via configuration of phased-array antennas, RF front ends, ADC, and DAC, while the edge processing provides reconfigurability via scalable inline processing. Using a mathematical model for processing time (the proposed figure of merit), we present results which show that mmMoReEdge is 50% to 70% faster as compared to an offline general-purpose processor based architecture and is 30% to 40% faster as compared to a node-based architecture with one FPGA.**

***Index Terms*—Software Defined Networks, Software Defined Radio, 5G, IoT, Edge Computing, Modular, Reconfigurable**

I. Introduction

The fifth generation (5G) cellular standard is being designed to support high-bandwidth and low-latency communication for a variety of applications including health, transportation, manufacturing, and public safety [1]. A key requirement to enable these use cases is the need for a modular and reconfigurable testbed for testing these applications in configurations that closely mimic real-world situations. A testbed typically consists of three subsystems, namely: the acquisition subsystem, the computing subsystem, and the application subsystem. The acquisition subsystem contains components such as antennas, RF up- and down-converters, analog-to-digital converters (ADC) and digital-to-analog converters (DAC). The computing subsystem contains the processors and interconnect devices needed for processing the acquired signals. Finally, the application subsystem is the central hub for data management and user interaction. Software defined radio (SDR) based testbeds can be classified into these six categories, depending on how the computing subsystem is structured [2],

- General-purpose processor (**GP**) approach: GP uses a central processing unit (CPU) based platform (PC) as the computing subsystem for offline processing. It provides flexibility and ease of use, but suffers from throughput constraints and non-real-time behavior due to the lack of determinism.
- Co-processor approach: This approach relies on the addition of a co-processor, such as a Graphical Processing Unit (GPU), to the GP approach to perform complex signal processing.
- Processor-centric approach: This approach uses dedicated processors for time-sensitive operations such as controlling TCP-IP layers. Conventional Digital Signal Processors (DSPs), special purpose (custom-built) processors, and hardware accelerators are used to aid the central processor.
- Configurable units approach: In order to provide low energy consumption, this approach substitutes DSPs with special-purpose configurable units.
- Programmable blocks (**PB**) approach: PB uses programmable blocks such as FPGAs with or without embedded processors. It provides great flexibility to create tailored architectures via run-time reconfigurability. Programmable blocks offer high computing power for moderate energy consumption.
- Distributed approach: Custom testbeds based on a distributed computing approach, where the complex signal processing is spread out to a farm of processing elements on the Internet.

Fig. 1 illustrates a simple application using cloud computing, on-premise computing, and edge computing (a key part of the 4-stage Internet of Things (IoT) solutions architecture [3]). Imagine two parking lots, P1 and P2, being monitored by a camera. In the case of cloud computing, there are no local processors in each parking lot. Instead, the images acquired by both cameras are sent to an external server (cloud) for feature extraction, database searches, and storage. In the case of on-premise computing, both P1 and P2 have their own dedicated processors which compute the information locally. Both of these techniques have challenges related to bandwidth

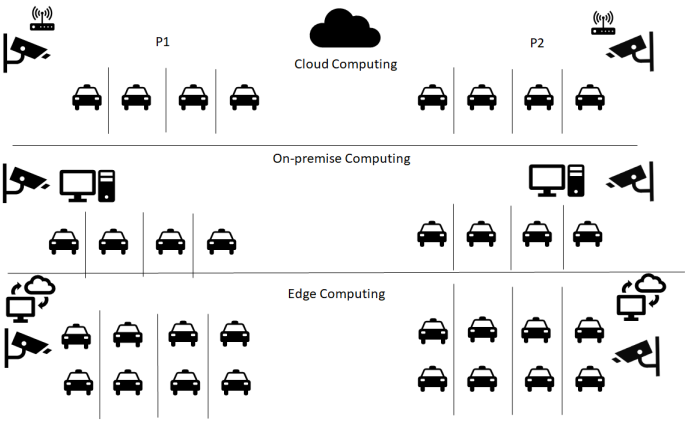

Fig. 1. A Simple Application Using Cloud Computing, On-premise computing, Edge Computing

utilization and localized optimization respectively, which are further exacerbated as the number of cars being monitored increases. Edge computing overcomes both of these challenges as it allows for computation, such as processing of feature extraction, to be performed locally. These results are then sent to the cloud server for object recognition, database searches, and information processing. In this way processing is distributed between the cloud and the node and data traffic is reduced.

In this paper, we use the principles of edge computing to propose mmMoReEdge, a testbed that offers run-time reconfigurability with online processing to enable mmWave 5G tests. Run-time reconfigurability at the software layer allows the system to adapt to different gain profiles, channel conditions, and antenna configurations. Modularity at the hardware level enables the acquisition and computing subsystems to leverage commercially-available components, thereby enabling the system to scale with evolving requirements. We compare the performance of mmMoReEdge with GP and PB approaches for different use cases representing low, medium, and high complexity signal processing and present model-based results for the same. The key contributions of this paper are:

- We present the system-level design of mmMoReEdge, a modular and reconfigurable testbed inspired by the edge computing architecture. We describe the interconnection between the key components of the testbed, namely the edge and the cluster of nodes.
- We present a mathematical model for the parameter *processing time*, which is used as the key figure of merit, to compare mmMoReEdge with the GP and PB architectures.
- We describe three different measurements, namely IQ Power, Complex FFT Spectrum, and Angle of Arrival as a representation for low, medium, and high complexity signal processing. Processing time for these three measurements is used as the figure of merit for comparing different architectures.
- We present results which demonstrate that mmMoReEdge outperforms the GP and PB approaches for medium- and high-complexity use cases. For example, mmMoReEdge is 50% to 70% faster as compared to the GP approach and is 30% to 40% faster as compared to the PB approach.

II. 5G Testbed Performance Metrics

The design of a testbed can be optimized around the vectors of throughput, hardware agility, scalability, cost, and latency [4], [5]. Throughput of a test system can be described as the ability to transmit and/or receive data at a desired rate. It is mainly driven by the real-time bandwidth of the radio front end, ADC sampling rates, heterogeneous processing, and bus architecture. Hardware agility can be described as the ability of a system to reconfigure its input at runtime, using parameters such as frequency, power level, and sampling rates. Scalability can be described as the ability of a testbed to extend its use for future applications without major re-design. Cost is usually measured as the total cost of ownership, which is a function of the purchase, development, and maintenance costs. Finally, latency is characterized by the speed and deterministic nature of processing. It is influenced mainly by two factors: the type of computing nodes used and the bus technology connecting the computing nodes.

The metric of latency is dependent on the transmit time, receive time, and decision-making time. For this evaluation performed in this paper, we have chosen, processing time, which is the amount of time it takes for the test system to make a decision based on acquired data, as the key figure of merit. For the purpose of comparing different testbed architectures, we model the processing time metric using (1):

$$T = t_a + \sum_{i=1}^{N} (S_i/B_i + M_i/(P_i * k_i)) \tag{1}$$

Here, we use the following notations:

- t_a is the acquisition time in seconds.
- S_i is the number of samples being transmitted between the source and sink node for a particular computing platform.
- B_i is the bandwidth in Samples/Second for the bus technology to transmit these samples, $B > 0$.
- M_i is the number of operations needed to make the decision.
- P_i is the processing power of the computing platform in operations/second, $P > 0$.
- k is a scaling factor based on the amount of available processing capability, $0.1 \leq k \leq 1.0$.
- N is the number of processors in the testbed.

A block diagram of testbeds using the GP approach and the PB approach is shown in Fig. 2 and Fig. 3 respectively. In this paper, we will compare the performance of the proposed mmMoReEdge testbed with these two architectures. In the GP architecture, there is no processor on the testbed node, a concept similar to the cloud computing use-case as shown in Fig 1. The only processor is on the PC. Hence, N is set to 1.

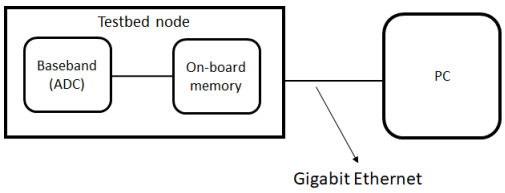

Fig. 2. General Purpose Processor Based Architecture

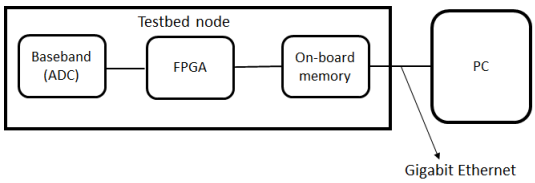

Fig. 3. Programmable Blocks Architecture

The data source is the on-node memory and the data sink is the memory on the PC. We assume a Gigabit Ethernet bus between the source and the sink. For the purpose of this comparison, we use a laptop with an Intel(R) Core(TM) i7-6820HQ, where the quad-core CPU is running at 2.70 GHz with 8 logical processors as the PC. We assume that the measurements will be run with highest priority on one core, thereby reducing the variability in the processing time. With these assumptions, we have set $N = 1$ and the values for different parameters in (1) as shown in Table I.

TABLE I
VALUES OF PARAMETERS FOR GENERAL PURPOSE CPU APPROACH

Parameter	PC
k	1.0
B	1e9
P	2.7e9

In the PB architecture, traditionally, there is one or more FPGA on the testbed node, in addition to the processor on the PC. This is similar to the concept of on-premise computing as shown in Fig 1. This single, on-node FPGA is used for both hardware configuration and any inline signal processing that needs to be performed. Hence, N is set to 2. The data source for the first processor is the ADC on the node and the data sink is the FPGA. The bus technology connecting these two nodes is typically a high-speed serial protocol such as Serial RapidIO (sRIO) or Aurora. The signaling rate for sRIO can be 1.25, 2.5, or 3.125 Gbps per differential transmit and receive pair. For FPGAs, we consider a configurable microprocessor/microcontroller architecture supported on most FPGA families, including the Zync7000 from Xilinx [6]. This supports a processing speed of 270 DMIPS (Dhrystone million instructions per second). However, between 50% to 90% of the FPGA resources may be utilized by the instrument provider for control and configuration, thereby leaving only a fraction of the resources for inline processing [7]. As an example, if 90% of the FPGA resources are used for control and configuration, then only 10% is available for processing, hence $k = 0.1$. The data source for the second processor is the on-node memory and the data sink is the memory on the PC. For our comparison, we will assume that the node only has one on-board FPGA. With these assumptions, we have set $N = 2$, and the values for different parameters in (1) are shown in Table II.

TABLE II
VALUES OF PARAMETERS FOR PROGRAMMABLE BLOCKS APPROACH

Parameter	Node	PC
k	0.1-0.5	1.0
B	2.5e9	1e9
P	270 DMIPS	2.7e9

Next, we describe three measurements, along with their use cases, that we have considered for evaluating the processing time metric. We have considered these three measurements as they represent low-, medium-, and high-complexity computations, respectively.

- IQ Power Measurements (Low-Complexity): As 5G emphasizes the need for radiated (over-the-air) signal tests, it is important to measure the Peak-to-Average Power Ratio (PAPR) of the received signal and operate the receiver within its linear operating range. A 5G testbed should have the ability to measure the PAPR of the incoming signal and adjust the operating power of the testbed to maximize dynamic range. This is typically done using the IQ power measurement calculations.
- Complex FFT Spectrum (Medium-Complexity): This measurement calculates the magnitude and phase (relative to a reference) of the signals as a function of frequency. For 5G and mmWave applications, measurements have to be done within the coherence time, wherein the channel state can be considered to be constant. Due to this, a 5G testbed should have the ability to make fast and repeatable measurements within a fixed time period.
- Angle of Arrival using MUSIC algorithm (High-Complexity): Directionality will be a key feature of 5G networks for beam forming/steering capabilities. To closely mimic real-world scenarios, a 5G testbed should be able to make angle of arrival measurements and use this information as control signals to adjust the RF front end for different beam parameters.

III. PROPOSED TESTBED SYSTEM DESIGN

In this section, we describe the system design of the proposed testbed, called mmMoReEdge, which consists of a cluster of multiple testbed nodes, the testbed edge, and the host PC, as shown in Fig. 4. This design has been inspired by edge computing, a distributed and open information technology (IT) architecture that features decentralized processing power. In this architecture, data is processed on a local processor in close promixity (called edge) of the node. Fig. 4 shows the system-level design of mmMoReEdge.

A group of testbed nodes can be used to form a cluster, wherein each node contains antennas that are attached to a

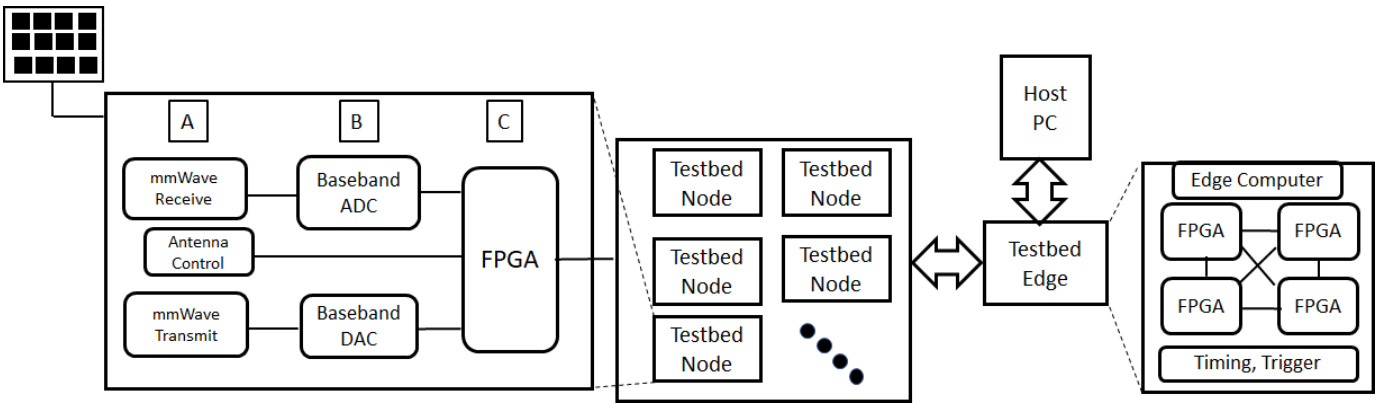

Fig. 4. mmMoReEdge, a mmWave MOdular and REconfigurable testbed inspired by Edge computing architecture.

mmWave subsystem (subsystem A) that allows for frequency translation to and from mmWave frequenices. The testbed has been designed to adapt to mmWave frequencies for multiple use-case [8]. The baseband (ADC, DAC) subsystem (subsystem B) operates at sub-6 GHz frequencies and manages the analog-to-digital and digital-to-analog conversion at wider bandwidths. The on-node FPGA (subsystem C) can be used for tasks such as hardware configuration, inline calibration, and antenna subsystem control.

To enable additional inline signal processing and fast measurements, rather than relying on the on-node FPGA, mmMoReEdge provides the concept of a testbed edge, similar to the concept of edge devices. The testbed edge aggregates data from a number of nodes and delivers additional inline processing power, as shown in Fig. 4. The testbed edge can have multiple FPGAs, all interconnected via high-speed serial transceivers. The communication mechanism between the nodes and the testbed edge is shown as cabled PCIe, but also can be adapted to high-speed serial I/O for high data rate applications. Networking is provided through Linux RT based edge computer, which communicates with the host PC for application-layer support and connectivity to other servers for data storage. With the assumption of one testbed node, one FPGA per testbed edge, and one PC, we have set the value of N to 3, and the values for different parameters in (1) as shown in Table III. On the testbed edge, we assume that only 10% of the FPGA is used for management, thereby leaving about 90% for inline processing, hence the value of $k = 0.9$

TABLE III
VALUES OF PARAMETERS FOR ONE CONFIGURATION OF PROPOSED DESIGN

Parameter	Node	Edge	PC
k	0.1-0.5	0.9	1.0
B	2.5e9	2e9	1e9
P	270 DMIPS	270 DMIPS	2.7e9

A practical implementation of the testbed edge can be demonstrated using the NI ATCA-3671, which features four user-programmable Virtex-7 690T FPGAs. It has four slots for both analog and high-speed serial I/O options. Inter-FPGA communication is achieved via high-speed serial transceivers, maintaining a maximum data rate of 12.5 Gb/s. It supports 16 lanes to adjacent FPGAs and 12 lanes to diagonal FPGAs [9].

Run-time reconfigurability of the hardware elements is a key feature of the testbed and enabled by the control and processing software running on the FPGAs. The testbed is programmable across all the PHY-MAC TCP-IP layers and the instrumentation layers via a well-defined Application Programming Interface (API). For example, the physical layer API is responsible for controlling the modulation scheme, symbol rate, filter type, channel response equalization filter taps, or coding parameters. It also monitors the received signal characteristics, such as RSSI, and provides feedback to the upper layers. The testbed has been designed such that it allows for real-time configuration of the radio layer parameters.

Flexibility at the baseband level is enabled via the use of Software Defined Radios (SDRs) such as USRP [10]. As an example, the NI-USRP 2944 supports 160 MHz instantaneous bandwidth with radio frequency range of 10 MHz to 6 GHz. The sub-6 GHz band serves as the baseband system of our testbed and provides frequency coverage and run-time reconfigurability for research on topics such as the LTE-to-5G migration, LTE-5G co-existence, and IoT applications. The modular nature of our testbed node's mmWave heads addresses the challenges related to different frequency bands being considered for various 5G applications [11], [12]. Many of the new 5G implementations will require beam steering on multiple beams. Hence, as advanced beamforming/steering technology is developed and integrated into new 5G designs, mmMoReEdge can be easily adapted using the Antenna Control subsystem in Fig. 4. It has been designed to support beam forming/steering on multiple beams using commercially available phased-array antennas [13]–[16].

IV. Evaluation Results

In this section, we present results that use the processing time required for the three measurements described in Section III to compare the performance of GP, PB, and mmMoReEdge testbeds. The processing time is calculated

as per (1) with values of different parameters as defined in Tables I, II, and III.

A. Processing Time for Different Measurements

The number of real-valued multiplications and additions required to perform a particular measurement is used to determine the value of M in (1). While additional operations may be involved, we assume that the real-valued multiplications and additions serve as a practical proxy for our comparison purposes. The IQ Power measurement, used for adjusting the gain and reference values on the RF front end, is modeled using (2).

$$P^2 = I^2 + Q^2 \tag{2}$$

Here, we use the following notations:

- P is the scaled power measurement.
- I is the value of the in-phase component
- Q is the value of the quadrature-phase component

As seen, it has two real-valued multiplications and one real-valued addition for each measurement sample. Hence, the value of M is set to 3 per measurement sample. The second measurement being used for comparison purposes is the Complex FFT Spectrum for magnitude and phase calculations. It has been shown that a complex FFT measurement has $4N - 2log_2{}^2N - 2log_2N - 4$ real-valued multiplications [17] and $O(N \log N)$ complex-valued additions [18]. Each complex-valued addition has two real-valued additions: one for the real part and the other for the imaginary part. Assuming large values of N, we approximate the value of M per measurement sample to be $4 + 2 * log_2 2$. For the final measurement being compared, namely the Angle of Arrival, the value of M is calculated using $a^2 * N$ number of multiplications and $a^2 * (N-1)$ number of additions [19], where a is the number of antenna elements and N is the number of samples. In this work, we assume that the number of antenna elements is set to 16. Using these values, M is set to 256 per measurement sample.

B. Results and Observations

Table IV shows the time taken (in microseconds) by each measurement on the three different testbed architectures, using the values of M as calculated above and the other parameters as shown in Tables I, II, and III.

TABLE IV
TIME (IN MICROSECONDS) FOR EACH MEASUREMENT ON DIFFERENT TESTBED ARCHITECTURES, $k = 0.3$ FOR PB

Measurement	GP	PB	mmMoReEdge
IQ Power	2.16	0.66	0.33
FFT	4.82	1.23	0.50
AoA	195.2	43.17	13.06

For the results shown in the above table, the value of k is assumed to be 0.3, which implies that only 30% of the FPGA resources are available for measurement, while the rest of the FPGA fabric is being used for hardware configuration. This is only applicable for the PB testbed. As demonstrated by the results, the proposed mmMoReEdge testbed outperforms the other two architectures for all the three cases. We observe that, while the speedup is marginal for low-complexity measurements (such as IQ Power), it increases significantly as the complexity of the measurement increases. Fig. 5 shows how the measurement time varies as a function of

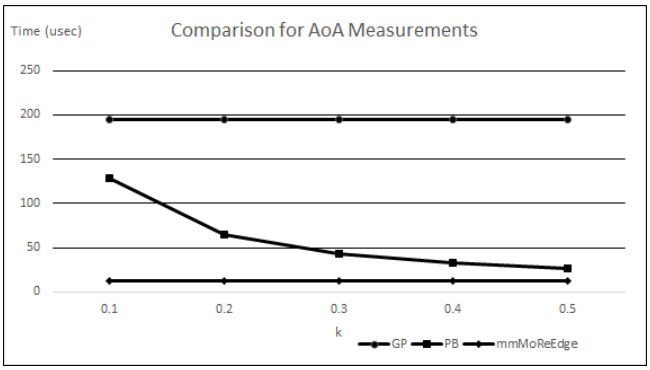

Fig. 5. Comparision of AoA measurements with different values of k

k for the Angle of Arrival measurement. We choose to present this measurement because it is the most complex of the three measurements. We vary values of k from 0.1 to 0.5, based on the assumption that, even in the best case, at least 50% of the FPGA resources will be used for hardware configuration. In other words, only 50% of the resources will be available for inline processing. Changing the value of k does not have an impact on the measurement times for GP and mmMoReEdge because these architectures do not rely on the FPGA on the node for processing.

Fig. 6 shows the performance comparison between PB (for two values of k) and mmMoReEdge, using the general purpose architecture as a baseline. Performance improvement P, as a percentage, is measured using (3).

$$P = \mid t_{gp} - t_i \mid / t_{gp} * 100, t_{gp} > 0 \tag{3}$$

Here, t_{gp} is the time taken for the measurement on a testbed with the general purpose architecture, and t_i is the time taken

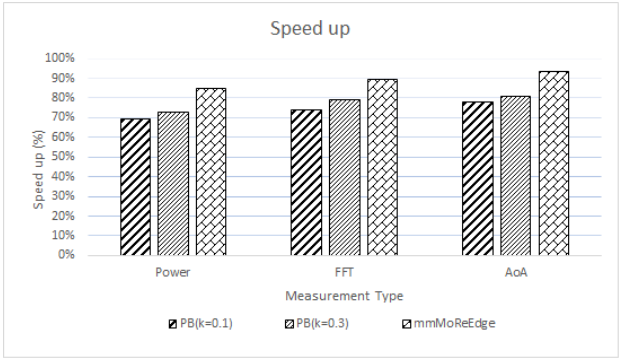

Fig. 6. Speedup Comparison using GP as baseline

for the measurement on a testbed with the architecture being compared, namely the proposed mmMoReEdge design and the programmable blocks architectures with values of $k = 0.3$ and $k = 0.1$. Our results indicate that mmMoReEdge is around $85\% - 93\%$ faster than the GP architecture, and the performance improvements are more pronounced as the complexity of the measurements increases. For $k = 0.3$, the proposed design is 50% faster for the IQ Power measurements, whereas it is 70% faster for the Angle of Arrival measurements.

V. Related Work

Existing 5G testbeds have been designed to meet the requirements of a specific application or achieve a particular learning outcome. They have been primarily designed for conductive (or cabled) stationary measurements and then, in some cases, adapted for mobile applications. The 5G CHAMPION testbeds [20] were designed for the 2018 Winter Olympic games to validate how 5G-enabled mmWave wireless backhaul can provide an inter-operable and seamless connection between two different access networks. The 5G Hardware Test Evaluation Platform [21] deploys software-defined wireless networks in an urban area, allowing academics, entrepreneurs, and wireless companies to test, evaluate, and improve their hardware design and software algorithms in a real-world environment. An approach focused on an educational setup for service-oriented process automation with 5G for emerging industrial technologies can be found in [22]. One testbed demonstrates SDN orchestration capabilities in adapting data paths across IoT, cloud, and network domains, based on the real-time load state of switches [23], enabling recovery from congestion, and assuring reliable data-delivery services. Each of these platforms have a high degree of specificity as to which applications they are built for, but less programmable than researchers might ultimately desire. POWDER [24] and COSMOS [25] projects, funded through the NSF PAWR initiative, are promising as they have been proposed emerging ideas for emerging mmWave frequency bands, different applications, and evolving specifications. Our work is an effort to take inspiration from the edge computing architectures on IoT devices and apply it for a modular and reconfigurable 5G testbed.

VI. Conclusion

This paper presents the design of mmMoReEdge, a modular and reconfigurable testbed based on a smart edge computing architecture. In this design, complex signal processing is performed on the testbed edge, which is a local cluster of processors in the close proximity of the testbed nodes. mmMoReEdge offers modularity via configuration of phased-array antennas, RF front ends, ADC, and DAC, while the edge processing capability provides run-time reconfigurability via scalable inline processing. A mathematical model for processing time, as the key figure of merit, is presented to evaluate different testbed architectures. Three different use cases, namely IQ Power measurements, FFT Power Spectrum, and Angle of Arrival measurements, are presented as examples of low, medium, and high complexity measurements respectively. The mathematical model results show that mmMoReEdge is 50% to 70% faster as compared to an offline CPU-based architecture and is 30% to 40% faster as compared to a node-based architecture with one FPGA.

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